IN THE CLAIMS

Claims 1-8 were pending in the current application. Claims 1-8 have been amended and new claim 9 has been added. A complete list of claims with amendments marked up is provided below:

1. (Currently amended) A method for current calibration of a plurality of I/O cells of an integrated circuit (IC) comprising:

setting a global control value ~~provided to the I/O cells~~;

providing the global value to the plurality of I/O cells to cause each of the plurality of I/O cells to output a logic voltage at a corresponding output pad; and

~~then,~~ for each I/O cell:

feeding back the logic voltage at the corresponding output pad to a comparator;

comparing the logic voltage at the corresponding output pad ~~of the I/O cell~~ with a reference voltage; and

~~sinking more current at the output pad by enabling additional driver bits associated with the I/O cell if the logic voltage is higher than the reference voltage; or~~

sinking ~~less~~ current at the corresponding output pad ~~by disabling additional driver bits associated with the I/O cell if the logic voltage is lower than the reference voltage~~based on result of the comparing.

2. (Currently amended) The method of claim 1, wherein ~~the~~ sinking ~~of more or less~~ current at the output pad comprises sinking current at the corresponding output pad ~~continues~~ until the logic voltage at the corresponding output pad and the reference voltage are substantially equal.

3. (Currently amended) The method of claim 1, wherein ~~the enabling/disabling of the additional driver bits is accomplished by modifying a local value stored in a register device associated with the I/O cell depending on the comparison of the logic voltage and the reference voltage~~sinking current at the corresponding output pad comprises:

enabling additional driver bits to sink more current at the corresponding output pad if the logic voltage is higher than the reference voltage; and

disabling additional driver bits to sink less current at the corresponding output pad if the logic voltage is lower than the reference voltage.

4. (Currently amended) The method of claim 3, wherein ~~the local value is modified by shifting 1s or 0s into the register device~~sinking current at the corresponding output pad comprises modifying a local value stored in a register device associated with a corresponding I/O cell based on the comparing of the logic voltage and the reference voltage.

5. (Currently amended) The method of claim ~~1~~4, wherein the register device ~~is~~ comprises a counter and the local value is modified by incrementing or decrementing the local value.

6. (Currently amended) A method comprising:

setting a global control value provided to ~~the~~ a plurality of I/O cells to cause each of the plurality of I/O cells to output a logic voltage on a corresponding output pad;

then, for each of the plurality of I/O cells:

feeding back the logic voltage at the corresponding output pad to a comparator;

setting a local value in a register device associated with the I/O cell in response to the global control value;

comparing the logic voltage ~~at the output pad of the I/O cell~~ with a reference voltage; and

setting a local value in a register device associated with a corresponding I/O cell in response to the global control value and result of the comparing of the logic voltage and the reference voltage.

~~sinking more current at the output pad by enabling additional driver bits associated with the I/O cell if the logic voltage is higher than the reference voltage; or~~

~~sinking less current at the output pad by disabling additional driver bits associated with the I/O cell if the logic voltage is lower than the reference voltage.~~

7. (Currently amended) The method of claim 6, ~~wherein the~~further comprising enabling ~~of the~~ additional driver bits ~~comprises modifying~~to modify the local value in the register device associated with the corresponding I/O cell in response to the comparison of the logic voltage and the reference voltage to sink more current at the corresponding output pad.

8. (Currently amended) The method of claim 6, ~~wherein the~~further comprising disabling ~~of the~~ additional driver bits ~~comprises modifying~~to modify the local value in the register device associated with the I/O cell in response to the comparison of the logic voltage and the reference voltage to sink less current at the corresponding output pad.

9. (New) The method of claim 4, further comprising shifting at least one of "1" and "0" into the register device to modify the local value.